

Preliminary Datasheet



Low Refresh Rate PLL IP Core targeted at Video and Flat Panel Display Applications

PRODUCT FEATURES

- > 15 KHz to 110 KHz Horizontal reference input
- > 13 MHz to 230 MHz Pixel Rate output clock
- > Multiplication ratios up to 4200
- > Peak to Peak Phase drift <1.6nS
- > Period Jitter 1-Sigma typical <14ps

Silicon Proven IP

All ParthusCeva PLL IP Cores are supported by evaluation platforms so Customers can test for themselves the quality of our IP. For our Low Refresh PLL IP Core we offer our 0.25um TSMC evaluation platform for customer verifications.

Introduction

ParthusCeva has developed a high performance PLL IP Core for use in Video and Flat Panel Display Applications that use the standard horizontal rate frequency to generate the required Pixel Rate Clock. Capable of accepting horizontal rate frequencies from 15 KHz to 110 KHz and providing pixel rates from 13 MHz to 230 MHz the ParthusCeva Low Refresh PLL can accommodate many standard modes including VGA, SVGA, XGA, SXGA, UXGA and a range of other modes. The core also includes a 16 step phase adjust mechanism used to deskew channels.

ParthusCeva's patented design controls phase drift maintaining typically <1ns input to output drift in most standard modes.

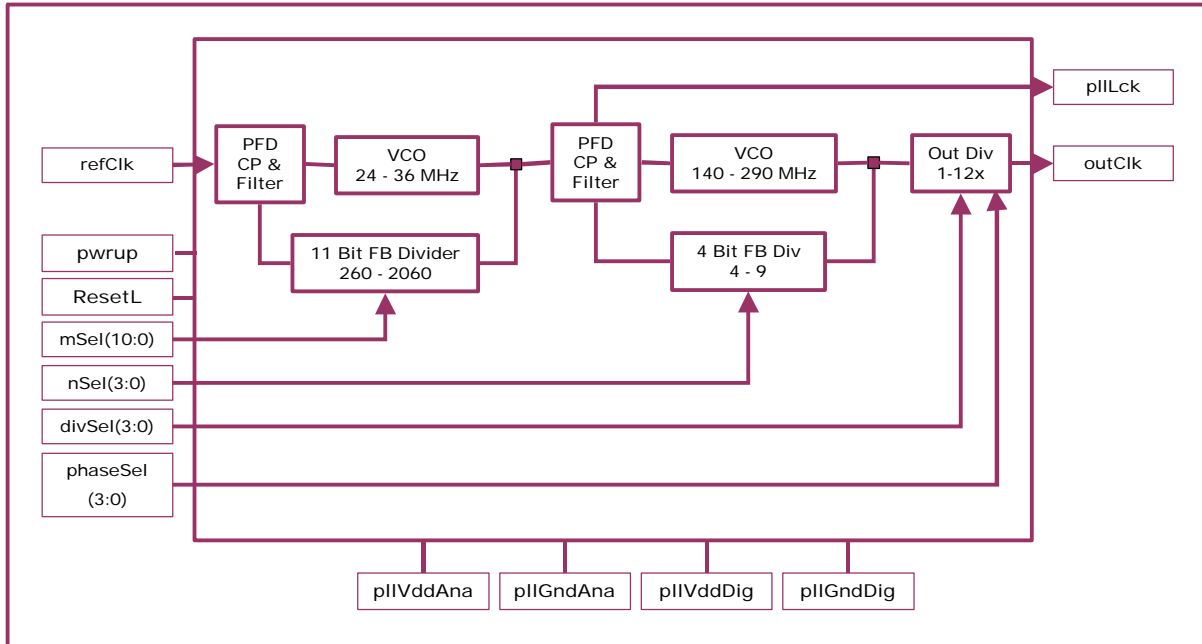
Proven in a number of processes including the TSMC 0.25um and a proprietary 0.13um IDM process the Low Refresh PLL has proved robust and portable across processes and geometry size.

ParthusCeva's PLL IP Cores have been licensed and used by our Customers in a wide range of applications and platforms leading to an unrivaled understanding of the system requirements for PLL performance. Parthus can accelerate your PLL design and can support your definition of the precise system requirements from the PLL.

Typical Specification for Low Refresh PLL

Parameter	Min	Typical	Max
Input Clock (Horizontal Freq) KHz	15		110
Output Clocks (Pixel Rate) MHz	13.5		229.5
Period Jitter Sigma [pS]*	10	14	25
Power [mW]	8	16	20
Power Supply [V]	2	2.5	2.7
Phase Drift (peak to peak) Input to output [nS]		1.6nS @30KHz Input	
Junction Temp [Deg]	0	-	125
Lock Time (mS)		1.75	
Phase Adjust mechanism		16 Steps along output clock period	

I/O Block Diagram and Pin Descriptions



Pin Descriptions

Signal Name	I/O	Comment
pllVddAna	I	2.5V Supply for PLL analog section
pllGndAna	I	Gnd for PLL analog section
pllVddDig	I	1.5V Supply for PLL digital section
pllGndDig	I	Gnd for PLL digital section
refClk	I	Input reference clock (1.5V)
resetL	I	Active Low Reset Signal (1.5V)
pwrup	I	Control to power up PLL (1.5V)
mSel<10:0>	I	Control Bus to select 1st stage divider value.
nSel<3:0>	I	Control Bus to select 2nd stage divider value.
divSel<3:0>	I	Control Bus to select 2nd Stage output divider value.
phaseSel<3:0>	I	Control for 16 step phase adjust
outClk	O	Overall PLL Output Clock (1.5/2.5 V)
pllLck	O	Indication PLL has acquired lock (1.5V)

Low Refresh Rate PLL Operating Modes

Mode	Resolution	Vertical Frequency KHz	Horizontal Frequency KHz	Multiplication Factor	Pixel Rate
VGA	640 x 480	60.00	31.5	800	25.175
VGA	640 x 480	72.00	37.9	832	31.500
VGA	640 x 480	75.00	37.5	840	31.500
VGA	640 x 480	85.00	43.3	832	36.000
SVGA	800 x 600	56.00	35.2	1024	36.000
SVGA	800 x 600	60.00	37.9	1056	40.000
SVGA	800 x 600	72.00	48.1	1040	50.000
SVGA	800 x 600	75.00	46.9	1056	49.500
SVGA	800 x 600	85.00	53.7	1048	56.250
XGA	1024 x 768	60.00	48.4	1344	65.000
XGA	1024 x 768	70.00	56.5	1328	75.000
XGA	1024 x 768	75.00	60.0	1312	78.750
XGA	1025 x 768	80.00	64.0	1336	85.500
XGA	1024 x 768	85.00	68.7	1376	94.500
SXGA	1280 x 1024	60.00	64.0	1688	108.000
SXGA	1280 x 1024	75.00	80.0	1688	135.000
SXGA	1280 x 1024	85.00	91.1	1728	157.500
UXGA	1600 x 1200	60.00	75.0	2160	162.000
UXGA	1600 x 1200	65.00	81.3	2160	175.500
UXGA	1600 x 1200	70.00	87.5	2160	189.000
UXGA	1600 x 1200	75.00	93.8	2160	202.500
UXGA	1600 x 1200	85.00	106.3	2160	229.500

Operating Modes

1. Operating modes are selectable by means of mSel, nSel and divSel control bus.
2. Alternative operating modes and frequencies beyond the scope of those listed above are supported. Consult ParthusCeva for other options if your requirements exceed those listed.

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Datasheet Revision 1.1