

# Advance Information



## 2.488GHz LC Tank PLL IP Core for SONET Applications

### PRODUCT FEATURES

- > 155.5 MHz Input Reference clock
- > 2.488GHz Output clock
- > Multiplication ratio 16x
- > 1-Sigma (RMS) Jitter <1pS
- > 1.2V Supply

Target Spec for LC Tank PLL

Parameter	Min	Typical	Max
Input Clock Frequency MHz		155.5	
Output Clock MHz		2488	
VCO Autocalibration		+/- 15%	
RMS Total Jitter (pS)		<1	
Power Supply (V)		1.2	
Power target mW		15	
Junction Temp [Deg]	0	-	100
Ambient Temp [Deg]	0	-	70

### Introduction

ParthusCeva has developed a high performance PLL using LC Tank architecture to achieve ultra low jitter. Applications such as SONET and Serial Communications have very low jitter requirements which often cannot be met using standard ring oscillator architectures.

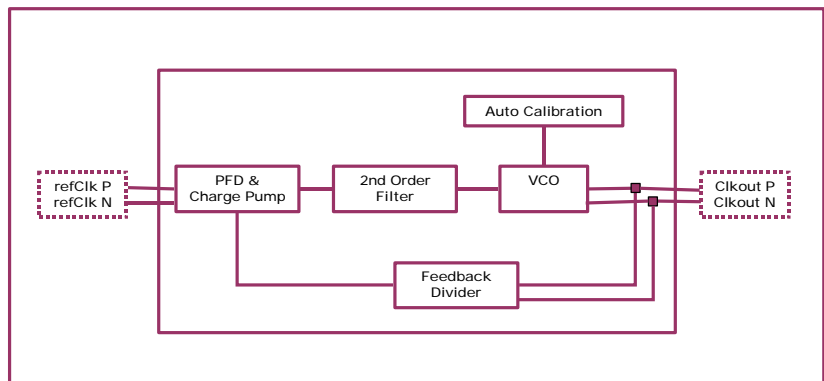
This initial designs has been targeted at the TSMC 0.13um process and operates at a 2.488GHz output clock rate. Other processes and other output clock rates can be designed on request.

ParthusCeva's PLL IP Cores have been licensed and used by our Customers in a wide range of applications and platforms leading to an unrivaled understanding of the system requirements for PLL performance. Through our experience ParthusCeva can accelerate your PLL design and can support your definition of the precise system requirements from the PLL.

### Silicon Proven IP

All ParthusCeva PLL IP Cores are supported by evaluation platforms which can be made available to Customers on completion of the IP development program.

### Block Diagram



ParthusCeva, Inc. PLL IP Business  
Unit 2, University Technology Center  
Curraheen Road, Cork, Ireland  
Tel: +353 21 480 1900 Fax: +353 21 480 1901

ParthusCeva, Inc. Headquarters  
2033 Gateway Place, Suite 150, San Jose, CA 95110-1002, USA  
Tel: +1 408 514 2900 Fax: +1 408 514 2995

ParthusCeva, Inc. Principal Offices  
5 Shenkar Street, P.O.Box 2019, Herzelia 46120, Israel  
Tel: +972 9 952 9788 Fax: +972 9 957 2898  
32-34 Harcourt Street, Dublin 2, Ireland  
Tel: +353 1 402 5700 Fax: +353 1 402 5711

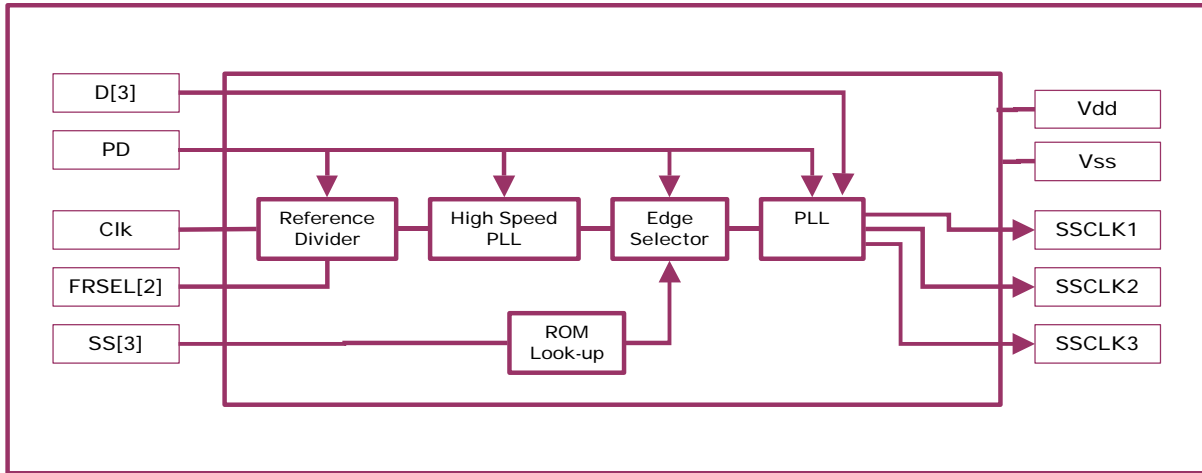
Info@parthusceva.com

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Datasheet Revision 1.0

## I/O Block Diagram and Pin Descriptions



### Pin Descriptions

Signal Name	Comment
VDD	Positive Power supply
VSS	Power supply Ground
CLK	Input clock (stable clock)
D[3]	Digital output clock scaling digital control input, see Table 1
FRSEL[2]	Input frequency range selection, digital control input, see Table 2.
SSCLK1	Output Spread spectrum clock. Table 1 for frequency programmability
SSCLK2	Output Spread spectrum clock. Table 1 for frequency programmability
SSCLK3	Output Spread spectrum clock. Table 1 for frequency programmability
PD	Active High power down pin
SS[3]	These pins control the depth and type of modulation see Table 3