



**Access our Compiler  
free of charge at  
[www.pllxpert.com](http://www.pllxpert.com)**

## Silicon based PLL Compiler

ParthusCeva's PLL Compiler is based on real measured silicon and offers the most robust, lowest risk PLL IP Core solution

### PRODUCT FEATURES

- > Integrated loop filter and band gap means no external components
- > Differential design provides excellent noise immunity
- > Compiler flexibility allows for deskew and 8 bit field programmable dividers
- > Datasheets, Verilog/VHDL behavioral models, Lib and Lef files for the PLL IP Core are generated and delivered automatically
- > PLL IP Core is delivered as optimized GDSII, DRC clean and CDL is supplied to facilitate LVS
- > You can design and deliver customized PLL IP Cores in minutes

### APPLICATIONS

- > Custom Clock Generation
- > Frequency multiplication
- > Multi-phase output control
- > Input buffer and clock tree de-skew
- > Duty cycle correction and control
- > Input Jitter reduction

## PLLXpert Online

### 0.18um PLL Design Compiler PLL IP for UMC

#### Introduction

PLLXpert Online is ParthusCeva's high performance online compiler for the design and delivery of PLL IP Cores.

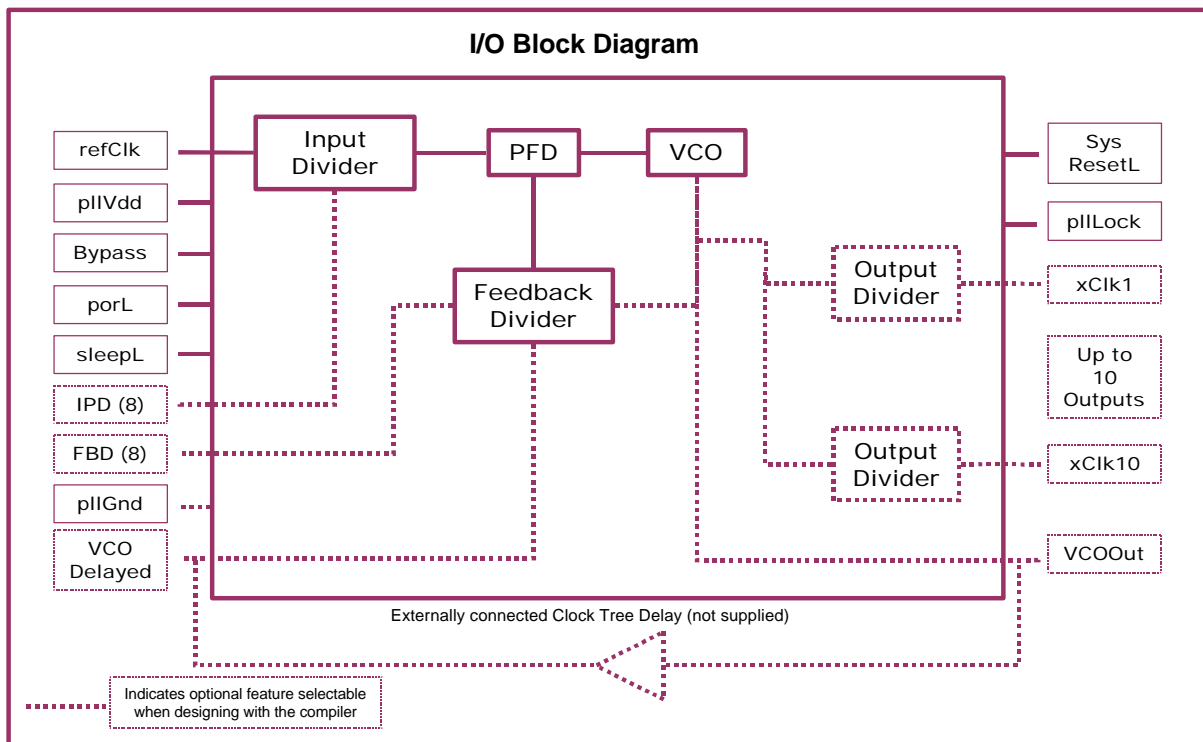
Integrated PLL's have become a critical feature in many of today's digital and mixed signal integrated circuit designs. Nonetheless they remain the most challenging technology block to develop in the digital IC, requiring a disproportionate amount of design and layout resources.

ParthusCeva's PLLXpert Online, simplifies all tasks associated with PLL design allowing the user to achieve a high performance, cost effective solution in minutes. State of the art designs can be produced without prior knowledge of PLL design theory by simply selecting a target process technology and defining the reference and output clocks, PLLXpert Online does the rest delivering datasheets, verilog, and GDS direct to the designers e-mail.

ParthusCeva's PLL IP Cores are used in all of our platform solutions and have also been licensed to many customers worldwide. Our PLL IP Cores are used in :-

- > Transceivers for gigabit serial communications
- > Processors with demanding low jitter requirements
- > GPS and mobile wireless communications
- > Fast DSP solutions for graphics and media processing.

Such platform level experience has lead to an unrivaled understanding of the system requirements for PLL performance. Parthus can accelerate your PLL design and can support your definition of the precise system requirements from the PLL.



## Pin Descriptions

Signal Name	Signal Type	Comment
refClk	Input:D	Input Clock
porL	Input:D	Power on reset. When low the block is reset, when high the block is active
VCOOut	Output:D	Buffered VCO Output
xClkn	Output:D	Output Clock(s)
forceBypass	Input:D	PLL Bypass. When High input clock is fed through to VCOOut
sysResetL	Output:D	Goes high on third positive edge of the slowest output clock after PIILock is first set following a PorL cycle. (During which the clocks are active). Will not deassert if PIILock subsequently indicates loss of lock.
pIILock	Output:D	Goes high when Phase Detector indicates lock for 32 successive cycles of reference clock. Will deassert subsequently if Phase Detector indicates loss of lock. Criterion for in lock/out of lock is programmed by PLLXpert s/w to change with input reference clock frequency
IPD(8)	Input:D(8)	IPD(8) is a static bus which must be set up at device power-up, capability of dividing between 1 and 256.
FBD(8)	Input:D(8)	FPD(8) is a static bus which must be set up at device power-up, capability of dividing between 1 and 256.
sleepL	Input:D	Turns off PLL when low.
pIIvdd	Power	Dedicated Vdd pin
pIIgnd	-	Dedicated Ground Pin

The above Block Diagram and Pin Description shows the complete I/O list including VCO Output, Programmable Dividers and Deskew Options. Compiler selectable options are shown as dotted lines. When these options are not selected the associated I/O is removed from the delivered IP

## Compiler Inputs

Parameter	UMC 0.18um Process			Description
	Min	Typical	Max	
Ref frequency [MHz]	0.5	Selectable	650	Ref Frequency / IPD = $f_{PFD}$ (Design center frequency of PFD). Note $f_{PFD}$ is limited to 0.5 MHz to 200MHz so in the event Ref frequency >200MHz an input pre-scaler is required by default
VCO frequency [MHz]	128	Selectable	650	Design center frequency of VCO $f_{VCO}$
Output Divider Ratios	2	Selectable	32	The VCO and up to 10 additional outputs are available each with a selectable 2 - 32 divide ratio w.r.t. VCO
Input Divider (IPD)	1	Programmable	256	Pre-scaler used to align the input RefClock to the PFD design frequency range. Divider can be fixed or field programmable via 8-bit bus.
Feedback Divider (FBD)	1	Programmable	256	Feedback Divider used to set multiplication factor $PFD * FBD$ ratio = $f_{VCO}$ . Divider can be fixed or field programmable via 8-bit bus.

## IP Core Electrical Specification

VCO frequency range <sup>Note 1</sup>	$f_{VCO} - 25\%$	$f_{VCO}$	$f_{VCO} + 25\%$	Selectable frequency range of the VCO if programmable dividers are enabled
PFD frequency range	$f_{PFD} - 25\%$	$f_{PFD}$	$f_{PFD} + 25\%$	Usable frequency range of the PFD.
Output frequency	$f_{VCO}/32$		$f_{VCO}$	Determined by Output Divider ratios selected during design
Jitter Sigma [pS]	3.5	6	16	Period Jitter Measurement (Histogram of cycle times)
DJs [pS] <sup>Note 2</sup>		25	40	Typical Quiet Vdd Deterministic Jitter
DJvdd(100mv)		120	140	Typical Deterministic Jitter for 100mV of noise @ 40MHz on Vdd
Power [mW]	7	11	15	Total power consumption of PLL
Power Supply [V]	1.6	1.8	2	Power Supply voltage (Vdd)
Loop Bandwidth [MHz]	0.1	0.8	3	Value obtained as a result of Input clock suppression and stability constraints
Junction Temp [Deg]	-20	27	125	Consult Parthus for additional information.
Phase Margin [Deg]	50			Guaranteed over process, voltage and temperature
Ref Clock Suppression [DB]	40			Necessary to suppress incoming jitter
Deskew, direct connection		300pS		Phase difference between refClk and VCOOut when VCOOut is directly connected to VCODelayed. Consult Parthus for additional information.
Deskew with FB Buffer		300ps+7% of I/P Buf Delay		Phase difference between refClk and VCOOut with Balancing Buffer in the feedback path. Consult Parthus for additional information.
Max Deskew Delay ns			0.02/BW	Maximum Dskew Delay that can be introduced into the feedback path. BW is Loop BW in MHz. Value supplied for each specific design in Online Datasheet

## Electrical Specification Notes

- Note that in ParthusCeva's 0.18um PLLs the Absolute Max VCO Frequency is 700 MHz (worst case temp and process). Any event that causes the VCO to be driven to higher than 700 MHz will require a POR to re-initialize the PLL.
- Deterministic Jitter  $Dj = DJs + [DJvdd * (Vddnoise/100mV)]$ .
- For more detailed specifications and applications information a datasheet is available for each specific PLL designed using PLLXpert Online.

## Design Options

- > Simple fixed integer PLLs minimizing the die area, complexity and power consumption of the device
- > More complex designs with 8 bit field programmable input and feedback dividers enabling Fractional-N capability
- > Up to 10 output clocks each with 5 bit divider resolution, which is selectable during the design
- > Deskew option opens the feedback path enabling the output to be deskewed with respect to the input clock

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