



eSILICON ANNOUNCES SUCCESSFUL DEPLOYMENT OF ASIC CHIP INCORPORATING PARTHUSCEVA PLL IP

San Jose, Calif - July 03, 2003 - ParthusCeva, Inc. (Nasdaq: PCVA, LSE: PCV) the leading licensor of Digital Signal Processor (DSP) cores, platform-level and PLL IP to the semiconductor industry, and eSilicon Corporation, a leading fabless custom chip company, today announced the successful deployment of an ASIC chip incorporating ParthusCeva's 0.13um PLL technology.

The ASIC is a 0.13um System-on-Chip comprising of an embedded processor core, USB and memory as well as ParthusCeva's 0.13um PLL. Fabricated on the TSMC 0.13um LV process, the chip was designed for a high volume ADSL modem application and is now in volume production.

"ParthusCeva offers an advanced and flexible approach to PLL design", said Jim Ensell, VP Business Development and CIO, eSilicon Corporation. "The technology delivered a first-time-reliable PLL to power our latest ADSL SoC and the team supported us through deployment on the new TSMC 0.13um LV process".

"The eSilicon PLL deployment is an excellent example of how our PLLXpert compiler can help customers to achieve fastest time-to-market" said Kieran Flynn, PLL Business Manager at ParthusCeva. "This silicon validation of all our PLLs ensures our customers achieve right-first-time performance."

PLL Business Unit of ParthusCeva, Inc.

ParthusCeva offers PLL IP Cores in 0.25um through 0.18um and 0.13um, to the very latest 90nm processes, from foundry partners including, TSMC, UMC, 1st Silicon, Silterra and a number of proprietary IDM foundries. In addition, application-specific PLLs are available for Clock Synthesis, Jitter Reduction, Deskew, and EMI reduction functions in Computer, Communications and Automotive applications.

In addition, through PLLXpert Online, a web based PLL compiler, designers can either create a custom PLL or alternatively download an existing PLL reference design that can be fine-tuned by the designer for a specific application. No prior training, in-depth PLL design knowledge or additional EDA tools are required. PLLXpert Online delivers a complete design kit including datasheets, verilog models, and the necessary files for logic synthesis, place and route. These deliverables enable the designer to fully validate the integration of the PLL into the IC by optimising the PLL until it meets system requirements with immediate GDSII

delivery on final demand. For more information, visit ParthusCeva's PLLXpert Online website at <http://www.pllxpert.com>.

About eSilicon

eSilicon Corporation is a full-service provider of custom chips to the world's leading electronics companies. Founded in 2000, the company's unique approach manages every step of the IC development process - from specification through manufacturing and delivery of packaged and tested parts. eSilicon offers value-added design and manufacturing expertise, with an ebusiness infrastructure that provides significant visibility, predictability and time-to-market advantages. Headquartered in Sunnyvale, CA with offices in Allentown, PA, and Murray Hill, NJ, eSilicon has approximately 80 employees.

For more information about eSilicon, visit <http://www.esilicon.com>

About ParthusCeva

Headquartered in San Jose, ParthusCeva (Nasdaq: PCVA) and (LSE: PCV) is the leading licensor of DSP and a leading provider of application-specific platform Intellectual Property (IP) to the semiconductor industry. ParthusCeva was created as a result of the combination of Parthus Technologies plc, a leading provider of application-specific platform IP, and Ceva, formerly the licensing division of DSP Group, the leading licensor of DSP cores.

For more information, visit us at <http://www.parthusceva.com>.

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ParthusCeva Safe Harbor Statement

This document contains "forward-looking statements", which are subject to certain risks and uncertainties that could cause actual results to differ materially from those stated. Any statements that are not statements of historical fact (including, without limitation, statements to the effect that the company or its management "believes," "expects," "anticipates," "plans" and similar expressions) should be considered forward-looking statements. Important factors that could cause actual results to differ from those indicated by such forward-looking statements include uncertainties relating to the ability of management to successfully integrate the operations of Parthus and Ceva, uncertainties relating to the acceptance of our DSP cores and semiconductor intellectual property offerings, continuing or worsening weakness in our markets and those of our customers, quarterly variations in our results, and other uncertainties that are discussed in the registration statement on Form S-1 and the most recent quarterly report on Form 10-Q of ParthusCeva (formerly called Ceva, Inc.), on file with the U.S. Securities and Exchange Commission.